

WHAT IS CLAIMED IS:

1. A switching device comprising:

a first connection terminal,

a second connection terminal,

5 a third connection terminal,

a pair of first direct-current blocking capacitive elements,

a first FET provided with a pair of main terminals, one of which is connected, via one of the first direct-current blocking capacitive elements, to the first connection terminal and the other of which is connected, via the other of the first direct-current blocking capacitive elements, to the second connection terminal, and

a pair of second direct-current blocking capacitive elements,

a second FET provided with a pair of main terminals, one of which is connected, via one of the second direct-current blocking capacitive elements, to the first connection terminal and the other of which is connected, via the other of the second direct-current blocking capacitive elements, to the third connection terminal,

wherein:

a channel type of the first FET is the same as a channel type of the second FET,

a first bias voltage is applied to a gate of the first FET,

a second bias voltage is applied to the pair of main terminals of the second FET, and

either one of voltages, which are respectively lower and higher than both a voltage derived from subtracting a gate threshold voltage of the first FET with a sign from the first bias voltage and a voltage derived from adding a gate threshold voltage of the second

FET with a sign to the second bias voltage, is applied to the pair of main terminals of the first FET and to a gate of the second FET as a first control voltage,

whereby the first FET and the second FET enter a conductive state and a cut off state in a complementary manner to allow switching between a first connection state and a second connection state, wherein, in the first connection state, the first connection terminal and the second connection terminal are electrically connected to each other and the first connection terminal and the third connection terminal are electrically disconnected from each other and, in the second connection state, the first connection terminal and the third connection terminal are electrically connected to each other and the first connection terminal and the second connection terminal are electrically disconnected from each other.

2. The switching device according to claim 1, wherein the first bias voltage, the second bias voltage, and the first control voltage have voltage values not less than a ground potential.

3. The switching device according to claim 1, wherein a frequency of signal input to and output from the first, second, and third connection terminals is not less than 100 MHz and not more than 75 GHz.

4. The switching device according to claim 3, wherein the frequency of signal input to and output from the first, second, and third connection terminals is not less than 100 MHz and not more than 10 GHz.

5. The switching device according to claim 1 further comprising a control voltage terminal for application of the first

control voltage, wherein the pair of main terminals of the first FET and the gate of the second FET are connected to the control voltage terminal.

6. The switching device according to claim 5, wherein the pair of main terminals of the first FET are connected to the control voltage terminal via first bias resistor elements, respectively.

7. The switching device according to claim 6, wherein a sum of the resistance values of the two first bias resistor elements is not less than 100 times and not more than 100,000 times the ON resistance of the first FET.

8. The switching device according to claim 7, wherein the sum of the resistance values of the two first bias resistor elements is not less than 1,000 times and not more than 100,000 times the ON resistance of the first FET.

9. The switching device according to claim 6 further comprising a bias voltage terminal, wherein the pair of main terminals of the second FET are connected to the bias voltage terminal via second bias resistor elements, respectively.

10. The switching device according to claim 9, wherein a sum of the resistance values of the two second bias resistor elements is not less than 100 times and not more than 100,000 times the ON resistance of the second FET.

11. The switching device according to claim 10, wherein the sum of the resistance values of the two second bias resistor elements is not less than 1,000 times and not more than 100,000 times the ON resistance of the second FET.

12. The switching device according to claim 1, wherein the first and second FETs are n-channel type FETs.

13. The switching device according to claim 1, wherein the first control voltage takes two values, one of which is a voltage equal
5 to the first bias voltage and the other of which is a voltage equal to the second bias voltage.

14. The switching device according to claim 1, wherein the first and second FETs are depletion type FETs.

15. The switching device according to claim 1, wherein both
10 the first FET and the second FET are formed by a compound semiconductor composed of a compound made up of at least one element selected from among Ga, In, and Al and at least one element selected from among As, P, and N.

16. The switching device according to claim 1 further
15 comprising a third FET and a fourth FET,
wherein:

one of a pair of main terminals of the third FET is connected,
via a third direct-current blocking capacitive element, to the second
connection terminal while the other of the main terminals of the
20 third FET is connected, via a fourth direct-current blocking
capacitive element or via the fourth direct-current blocking
capacitive element and a first termination resistor element, to
ground,

one of a pair of main terminals of the fourth FET is connected,
25 via a fifth direct-current blocking capacitive element, to the third
connection terminal while the other of the main terminals of the
fourth FET is connected, via a sixth direct-current blocking

capacitive element or via the sixth direct-current blocking capacitive element and a second termination resistor element, to ground,

a channel type of the third FET is the same as a channel type of the fourth FET,

5 a third bias voltage is applied to a gate of the fourth FET,

a fourth bias voltage is applied to the pair of main terminals of the third FET, and

either one of voltages, which are respectively lower and higher than both a voltage derived from subtracting a gate threshold

10 voltage of the fourth FET with a sign from the third bias voltage and a voltage derived from adding a gate threshold voltage of the third FET with a sign to the fourth bias voltage, is applied, as a second control voltage, to the pair of main terminals of the fourth FET and to a gate of the third FET in synchronization with the first control
15 voltage,

whereby a group of the first and fourth FETs and a group of the second and third FETs enter the conductive state and the cut off state in a complementary manner, thereby the third connection terminal is terminated in the first connection state and the second
20 connection terminal is terminated in the second connection state.

17. The switching device according to claim 16, wherein the first control voltage is applied as the second control voltage.

18. The switching device according to claim 16,
wherein:

25 the first bias voltage is applied as the third bias voltage, and the second bias voltage is applied as the fourth bias voltage.

19. The switching device according to claim 1 further comprising a transmission line, having a second transmission signal terminal at one end thereof and a third transmission signal terminal at the other end thereof, for transmitting transmission signal,

5 wherein:

the first and second FETs are connected, via the transmission line, to the first connection terminal and the second and third connection terminals are connected to ground,

the first connection terminal is connected to a connection point
10 on the transmission line, and the first FET is connected, via the first direct-current blocking capacitive element, to a first point on the transmission line which is located a distance corresponding to odd-numbered times the quarter-wavelength of the transmission signal apart from the connection point of the first connection terminal
15 toward the second transmission signal terminal while the second FET is connected, via the second direct-current blocking capacitive element, to a second point on the transmission line which is located a distance corresponding to odd-numbered times the quarter-wavelength of the transmission signal apart from the connection
20 point of the first connection terminal toward the third transmission signal terminal,

the first connection terminal constitutes a first transmission signal terminal, and

in response to switching between the first connection state and
25 the second connection state, switching between a first transmission signal connection state and a second transmission signal connection state is established, wherein, in the first transmission signal

connection state, the first transmission signal terminal and the second transmission signal terminal are connected to each other to allow the transmission signal be transmitted and the first transmission signal terminal and the third transmission signal terminal are disconnected from each other not to allow the transmission signal be transmitted and, in the second transmission signal connection state, the first transmission signal terminal and the third transmission signal terminal are connected to each other to allow the transmission signal be transmitted and the first transmission signal terminal and the second transmission signal terminal are disconnected from each other not to allow the transmission signal be transmitted.

20. The switching device according to claim 19, wherein a frequency of signal input to and output from the first, second, and third transmission signal terminals is not less than 100 MHz and not more than 75 GHz.

21. The switching device according to claim 20, wherein the frequency of signal input to and output from the first, second, and third transmission signal terminals is not less than 100 MHz and not more than 10 GHz.

22. The switching device according to claim 19 further comprising a third FET and a fourth FET,

wherein:

one of a pair of main terminals of the third FET is connected, via a third direct-current blocking capacitive element, to a third point which is located a distance corresponding to odd-numbered times the quarter-wavelength of the transmission signal apart from

the first point toward the second transmission signal terminal on the transmission line, while the other of the main terminals of the third FET is connected, via a fourth direct-current blocking capacitive element or via the fourth direct-current blocking capacitive element and a first termination resistor element, to ground, and the ON resistance of the third FET or the sum of the ON resistance of the third FET and the resistance of the first termination resistor element is substantially the same as a characteristic impedance of the transmission line,

one of a pair of main terminals of the fourth FET is connected, via a fifth direct-current blocking capacitive element, to a fourth point which is located a distance corresponding to odd-numbered times the quarter-wavelength of the transmission signal apart from the second point toward the third transmission signal terminal on the transmission line, while the other of the main terminals of the fourth FET is connected, via a sixth direct-current blocking capacitive element or via the sixth direct-current blocking capacitive element and a second termination resistor element, to ground, and the ON resistance of the fourth FET or the sum of the ON resistance of the fourth FET and the resistance of the second termination resistor element is substantially the same as the characteristic impedance of the transmission line,

a channel type of the third FET is the same as a channel type of the fourth FET,

a third bias voltage is applied to a gate of the third FET,
a fourth bias voltage is applied to the pair of main terminals of the fourth FET, and

either one of voltages, which are respectively lower and higher than both a voltage derived from subtracting a gate threshold voltage of the third FET with a sign from the third bias voltage and a voltage derived from adding a gate threshold voltage of the fourth
5 FET with a sign to the fourth bias voltage, is applied, as a second control voltage, to the pair of main terminals of the third FET and to a gate of the fourth FET in synchronization with the first control voltage,

whereby a group of the first and third FETs and a group of
10 the second and fourth FETs enter the conductive state and the cut off state in a complementary manner, thereby, in the first transmission signal connection state, the second point is grounded and the fourth point is terminated and, in the second transmission signal connection state, the first point is grounded and the third
15 point is terminated.

23. The switching device according to claim 22, wherein the first control voltage is applied as the second control voltage.

24. The switching device according to claim 12,
wherein:

20 the first bias voltage is applied as the third bias voltage, and the second bias voltage is applied as the fourth bias voltage.